WE CLAIM:

1. A semiconductor structure comprising:

a monocrystalline silicon substrate;

an amorphous oxide material overlying the monocrystalline silicon substrate;

a monocrystalline perovskite oxide material overlying the amorphous oxide material; and

a monocrystalline compound semiconductor material overlying the monocrystalline perovskite oxide material, wherein the monocrystalline compound semiconductor material is piezoelectric.

2. The semiconductor structure of claim 1 further comprising at least one conductive element in contact with the monocrystalline compound semiconductor material.

3. The semiconductor structure of claim 1 wherein the monocrystalline compound semiconductor material is selected from the group consisting of gallium arsenide and aluminum gallium arsenide.

4. The semiconductor structure of claim 1 wherein the monocrystalline compound semiconductor material thickness is between about 0.05 μm and 100 μm.

5. The semiconductor structure of claim 1 wherein the monocrystalline compound semiconductor material thickness is between about 0.5 μm and 10 μm.

6. The semiconductor structure of claim 1 wherein the monocrystalline compound semiconductor material creates a reflective surface.

7. The semiconductor structure of claim 1 further comprising a reflective material overlying the monocrystalline compound semiconductor material.

8. The semiconductor structure of claim 6 further comprising an integrally formed electrical component in communication with the reflective surface of the monocrystalline compound semiconductor material.

9. The semiconductor structure of claim 7 further comprising an integrally formed electrical component in communication with the reflective material overlying the monocrystalline compound semiconductor material.

10. A semiconductor structure comprising:

a monocrystalline silicon substrate;

an amorphous oxide material overlying the monocrystalline silicon substrate;

a monocrystalline perovskite oxide material overlying the amorphous oxide material;

a monocrystalline compound semiconductor material overlying the monocrystalline perovskite oxide material; and

a piezoelectric material overlying the monocrystalline compound semiconductor material.

11. The semiconductor structure of claim 10 further comprising at least one conductive element in contact with the piezoelectric material.

12. The semiconductor structure of claim 10 wherein the piezoelectric material is selected from the group consisting of piezoelectric monocrystalline semiconductor material and piezoelectric monocrystalline ceramic material.

13. The semiconductor structure of claim 12 wherein the piezoelectric monocrystalline semiconductor material is selected from the group consisting of gallium arsenide and aluminum gallium arsenide.

14. The semiconductor structure of claim 12 wherein the piezoelectric monocrystalline ceramic material is selected from the group consisting of barium titanate, lead titanate, potassium niobate, lead niobate, and lead zirconate titanate.

15. The semiconductor structure of claim 13 wherein the piezoelectric monocrystalline semiconductor material thickness is between about 0.05 μm and 100 μm.

16. The semiconductor structure of claim 13 wherein the piezoelectric monocrystalline semiconductor material thickness is between about 0.5 μm and 10 μm.

17. The semiconductor structure of claim 14 wherein the piezoelectric ceramic material thickness is between about 0.5 μm and 200 μm.

18. The semiconductor structure of claim 14 wherein the piezoelectric ceramic material thickness is between about 5 μm and 25 μm.

19. The semiconductor structure of claim 10 wherein the piezoelectric material creates a reflective surface.

20. The semiconductor structure of claim 10 further comprising a reflective material overlying the piezoelectric material.

21. The semiconductor structure of claim 19 further comprising an integrally formed electrical component in communication with the reflective surface of the piezoelectric material.

22. The semiconductor structure of claim 20 further comprising an integrally formed electrical component in communication with the reflective material overlying the piezoelectric material.

23. A process for fabricating a semiconductor structure comprising:

providing a monocrystalline silicon substrate;

depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;

forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate; and

epitaxially forming a monocrystalline compound semiconductor layer overlying the monocrystalline perovskite oxide film, wherein the monocrystalline compound semiconductor layer is piezoelectric.

24. The process of claim 23 further comprising depositing at least one conductive element in contact with the monocrystalline compound semiconductor layer.

25. The process of claim 23 wherein the material to epitaxially form the monocrystalline compound semiconductor layer is selected from the group consisting of gallium arsenide and aluminum gallium arsenide.

26. The process of claim 23 wherein the monocrystalline compound semiconductor layer is formed to a thickness between about 0.05 μm and 100 μm.

27. The process of claim 23 wherein the monocrystalline compound semiconductor layer is formed to a thickness between about 0.5 μm and 10 μm.

28. The process of claim 23 wherein the monocrystalline compound semiconductor layer is formed with a reflective surface.

29. The process of claim 23 further comprising adhering a reflective material to the monocrystalline compound semiconductor layer.

30. The process of claim 28 further comprising integrating an electrical component with the monocrystalline compound semiconductor layer wherein the electrical component is in communication with the reflective surface.

31. The process of claim 29 further comprising integrating an electrical component with the monocrystalline compound semiconductor layer wherein the electrical component is in communication with the reflective material.

32. A process for fabricating a semiconductor structure comprising:

providing a monocrystalline silicon substrate;

depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;

forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate; and

epitaxially forming a monocrystalline compound semiconductor layer overlying the monocrystalline perovskite oxide film; and

forming a piezoelectric material layer overlying the monocrystalline compound semiconductor layer.

33. The process of claim 32 further comprising depositing at least one conductive element in contact with the piezoelectric material layer.

34. The process of claim 32 wherein the material to form the piezoelectric material layer is selected from the group consisting of piezoelectric monocrystalline semiconductor material and piezoelectric monocrystalline ceramic material.

35. The process of claim 34 wherein the piezoelectric monocrystalline semiconductor material is selected from the group consisting of gallium arsenide and aluminum gallium arsenide.

36. The process of claim 34 wherein the piezoelectric monocrystalline ceramic material is selected from the group consisting of barium titanate, lead titanate, potassium niobate, lead niobate, and lead zirconate titanate.

37. The process of claim 34 wherein the piezoelectric monocrystalline semiconductor material is formed to a thickness between about 0.05 μm and 100 μm.

38. The process of claim 34 wherein the piezoelectric semiconductor material is formed to a thickness between about 0.5 μm and 10 μm.

39. The process of claim 34 wherein the piezoelectric monocrystalline ceramic material is formed to a thickness between about 0.5 μm and 200 μm.

40. The process of claim 34 wherein the piezoelectric ceramic material is formed to a thickness between about 5 μm and 25 μm.

41. The process of claim 32 wherein the piezoelectric material layer is formed with a reflective surface.

42. The process of claim 32 further comprising adhering a reflective material to the piezoelectric material layer.

43. The process of claim 41 further comprising integrating an electrical component with the piezoelectric material layer wherein the electrical component is in communication with the reflective surface.

44. The process of claim 42 further comprising integrating an electrical component with the monocrystalline compound semiconductor material wherein the electrical component is in communication with the overlying reflective material.

45. A system for fabricating a semiconductor structure comprising:

means for providing a monocrystalline silicon substrate;

means for depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;

means for forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate; and

means for epitaxially forming a monocrystalline compound semiconductor layer overlying the monocrystalline perovskite oxide film, wherein the monocrystalline compound semiconductor layer is piezoelectric.

46. The system of claim 45 further comprising means for depositing at least one conductive element in contact with the monocrystalline compound semiconductor layer.

47. The system of claim 45 further comprising means for adhering a reflective material to the monocrystalline compound semiconductor layer.

48. The system of claim 45 further comprising means for integrating an electrical component with the monocrystalline compound semiconductor layer.

49. The system of claim 47 further comprising means for integrating an electrical component with the monocrystalline compound semiconductor layer wherein the electrical component is in communication with the reflective material.

50. A system for fabricating a semiconductor structure comprising:

means for providing a monocrystalline silicon substrate;

means for depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;

means for forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate; and

means for epitaxially forming a monocrystalline compound semiconductor layer overlying the monocrystalline perovskite oxide film; and

means for forming a piezoelectric material layer overlying the monocrystalline compound semiconductor layer.

51. The system of claim 50 further comprising means for depositing at least one conductive element in contact with the piezoelectric material layer.

52. The system of claim 50 further comprising means for adhering a reflective material to the piezoelectric material layer.

53. The system of claim 50 further comprising means for integrating an electrical component with the piezoelectric material layer.

54. The system of claim 52 further comprising means for integrating an electrical component with the monocrystalline compound semiconductor material wherein the electrical component is in communication with the overlying reflective material.